Claim Amendments:

1. (withdrawn) A method for manufacturing a block alterable memory cell, such method comprises the following steps:

depositing a screen oxide over a substrate layer;

depositing a mask implant layer over the screen oxide layer;

implanting memory cells in the portion of the substrate layer not covered by the mask implant layer;

etching a screen oxide and an initial gate oxide from memory cells;

depositing tunnel window mask;

etching a tunnel oxide layer;

depositing control poly layer; and

implanting source and drain regions.

2. (withdrawn) The method for manufacturing a block alterable memory cell of claim 1, wherein the step of deposing a control poly layer further comprising:

depositing a first oxide layer;

depositing an inter poly layer;

depositing a second oxide layer.

3. (withdrawn) The method for manufacturing a block alterable memory cell of claim 1, wherein said tunnel oxide layer having a thickness of 50-70 angstroms.

4. (withdrawn) The method for manufacturing a block alterable memory cell of claim 1, wherein said screen oxide layer having a thickness of 200-350 angstroms.

5. (currently amended) A block alterable memory cell, comprising:

a substrate layer having a source implant region, an active region, a floating gate transistor region, and a drain implant region;

a tunnel oxide layer ~~overlying~~ overlaying a portion of said substrate layer;

a first layer ~~overlying~~ overlaying said tunnel oxide layer;

an inter poly layer ~~overlying over~~ overlaying said first ~~oxide~~ layer; and

a second layer extending over said floating gate transistor region and said active region to an edge of said drain implant region.

6. (currently amended) The block alterable memory cell of claim 5, wherein ~~the~~ said substrate layer is a ~~p type doping~~ p-type doped substrate.

7. (currently amended) The block alterable memory cell of claim 5, wherein ~~the~~ said source implant region, said drain implant region, and said floating gate transistor region are ~~n type~~ n-type implants.

8. (currently amended) The block alterable memory cell of claim 5, wherein ~~the~~ said first layer is polysilicon and said second layer is ~~are~~ oxide ~~layers~~.

9. (currently amended) The block alterable memory cell of claim 5, wherein ~~the~~ said inter poly layer is a nitride layer.

10. (currently amended) The block alterable memory cell of claim 5, wherein ~~the~~ said substrate layer further comprises a thin surface layer.

11. (currently amended) A semiconductor memory device, comprising:

a memory array arranged into a plurality of rows and a plurality of columns[[;]], said memory array further comprising a plurality of block alterable memory cells, each block alterable memory cell having a substrate layer with a source implant region, an active region, a floating gate transistor region, a drain implant region, a tunnel oxide layer overlaying a portion of said substrate layer, a first layer overlaying said tunnel oxide layer, an inter poly layer overlaying said first layer, and a second layer extending over said floating gate transistor region and said active region to an edge of said drain implant region;

an input/output port in communication with said memory array; and

a controller coupled to said input/output port and said memory array[[;]].

~~wherein said memory array further comprising a plurality of block alterable memory cells, each block alterable memory cell further comprising:~~

~~a substrate layer having a source implant region, an active region, a floating gate transistor region, and a drain implant region;~~

~~a tunnel oxide layer overlying said substrate layer;~~

~~a first layer overlying said tunnel oxide layer;~~

~~an inter poly layer overlying over said first oxide; and~~

~~a second layer extending over said floating gate transistor region and said active region to an edge of said drain implant region~~.

12. (new) The block alterable memory cell of claim 5, wherein said inter poly layer is an ONO layer.

13. (new) A block alterable memory cell, comprising:

a substrate layer having a source doped region, an active region, a floating gate transistor region, and a drain doped region;

a tunnel oxide layer overlaying a portion of said substrate layer;

a first layer overlaying said tunnel oxide layer;

an inter poly layer overlaying said first layer; and

a second layer extending over said floating gate transistor region and said active region to an edge of said drain doped region.

14. (new) The block alterable memory cell of claim 13, wherein said substrate layer is a p-type doped substrate.

15. (new) The block alterable memory cell of claim 13, wherein said source doped region, said drain doped region, and said floating gate transistor region have n-type dopants.

16. (new) The block alterable memory cell of claim 13, wherein said first layer is polysilicon and said second layer is oxide.

17. (new) The block alterable memory cell of claim 13, wherein said inter poly layer is a nitride layer.

18. (new) The block alterable memory cell of claim 13, wherein said inter poly layer is an ONO layer.

19. (new) The block alterable memory cell of claim 13, wherein said substrate layer further comprises a thin surface layer.

20. (new) A semiconductor memory device, comprising:

a memory array arranged into a plurality of rows and a plurality of columns, said memory array further comprising a plurality of block alterable memory cells, each block alterable memory cell having a substrate layer with a source doped region, an active region, a floating gate transistor region, a drain doped region, a tunnel oxide layer overlaying a portion of said substrate layer, a first layer overlaying said tunnel oxide layer, an inter poly layer overlaying said first layer, and a second layer extending over said floating gate transistor region and said active region to an edge of said drain doped region;

an input/output port in communication with said memory array; and

a controller coupled to said input/output port and said memory array.

21. (new) A semiconductor memory device, comprising:

a memory array arranged into a plurality of rows and a plurality of columns, said memory array further comprising a plurality of block alterable memory cells, each block alterable memory cell having a substrate layer with a source doped region, an active region, a floating gate transistor region, a drain doped region, a tunnel oxide layer overlaying a portion of said substrate layer, a first layer overlaying said tunnel oxide layer, an inter poly layer overlaying said first layer, and a second layer extending over said floating gate transistor region and said active region to an edge of said drain doped region; and

an input/output port in communication with said memory array.